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## EUROPEAN PATENT APPLICATION

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### (54) Baseband predistortion system for linearising power amplifiers.

(57) The present invention concerns a predistortion system for amplifier linearisation characterised by the fact that it comprises a predistortion circuit in cascade to a clipping circuit composed of at least one clipping

device followed by at least one post-clipping filter device.

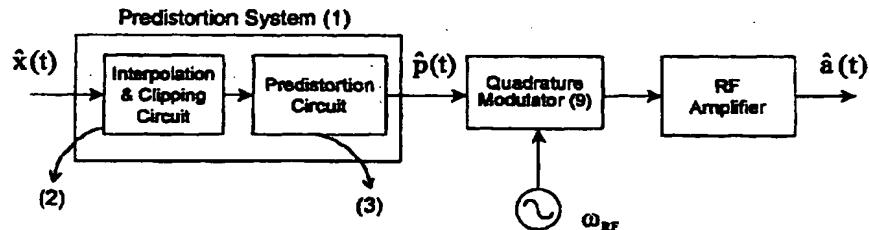


Fig. 1(a)

the output  $\hat{a}(t)$  of the amplifier.

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## Claims

1. A predistortion system for amplifier linearisation characterised by the fact that it comprises a predistortion circuit (3) in cascade to a clipping circuit (5) composed of at least one clipping device (5a) followed by at least one post-clipping filter device (5b).
2. According to claim 1, a system characterised by the fact that it employs at least one predistortion table (6).
3. According to claim 1, a system characterised by the fact that it employs at least one interpolation circuit (4) of the signal.
4. According to claim 3, a system characterised by the fact that the interpolation circuit is realised through a circuit (4a) for the insertion of zeros or replica of the first sample between successive samples of the signal, with the circuit (4a) that is followed by an interpolation filters circuit (4b) or (4c).
5. According to claim 3, a system characterised by the fact that the clipping device (5a) is positioned before the interpolation circuit (4) and in which the post-clipping filters device (4c) acts as interpolation filters.
6. According to claim 3, a system characterised by the fact that the clipping circuit (5) is positioned after the interpolation circuit (4).
7. According to claim 2, a system characterised by the fact that it employs an adaptation circuit (10) composed of a synchronisation circuit (8) at least and of an error circuit (7) which generates one error signal at least in order to update the predistortion tables (6).
8. According to claim 2, a system characterised by the fact that the predistortion tables (6) are addressed by the signal at the input of the predistortion circuit (3).
9. According to claim 1, a system characterised by the fact that clipping device (5a) limits the envelope of the signal, leaving its phase unchanged.
10. According to claim 1, a system characterised by the fact that the clipping device (5a) separately limits the two Cartesian components of the signal, therefore limiting its envelope and altering its phase.
11. According to claim 7, a system characterised by the fact that the error circuit (7) generates at least one of the error signal by the subtraction of the envelope and the phase of the amplifier baseband output signal from the corresponding components, at most scaled by a multiplicative coefficient, at the input to the predistortion circuit (3).

12. According to claim 7, a system characterised by the fact that each error signal is multiplied by at least one weighting coefficient.
- 5      13. According to claim 7, a system characterised by the fact that each value of the predistortion tables (6) is updated, for each value of their address, by summing to their original content the value of the error signal or a temporal mean performed on a number of values, that is greater or equal to one, that are consecutively assumed by the error signal for each address value.

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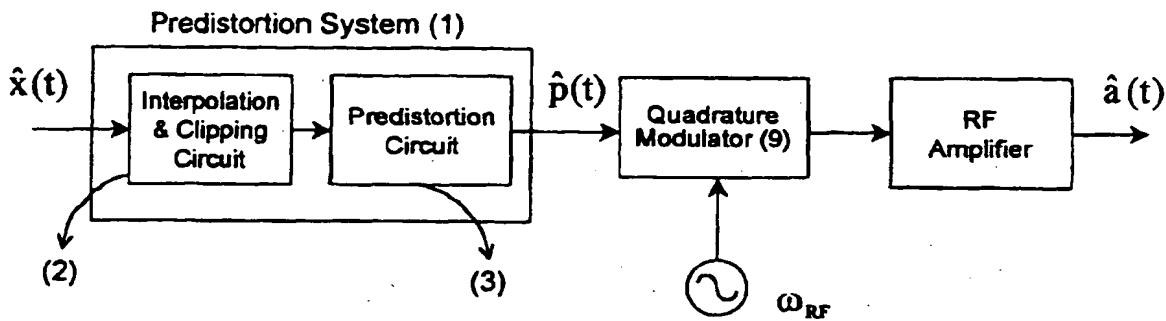


Fig. 1(a)

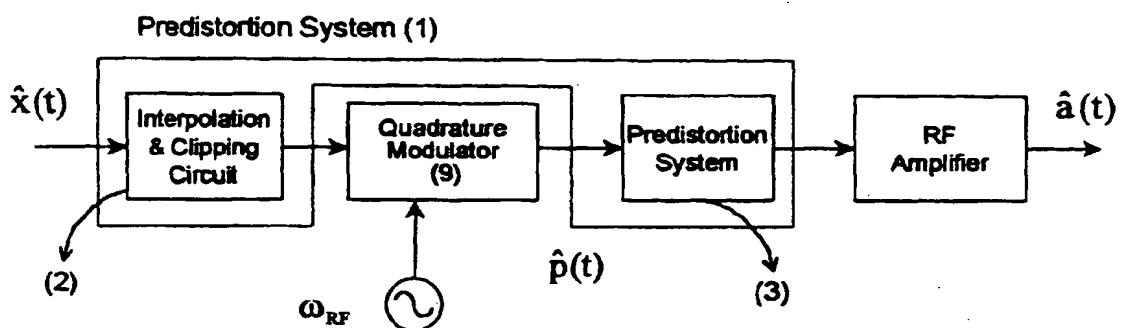


Fig. 1(b)

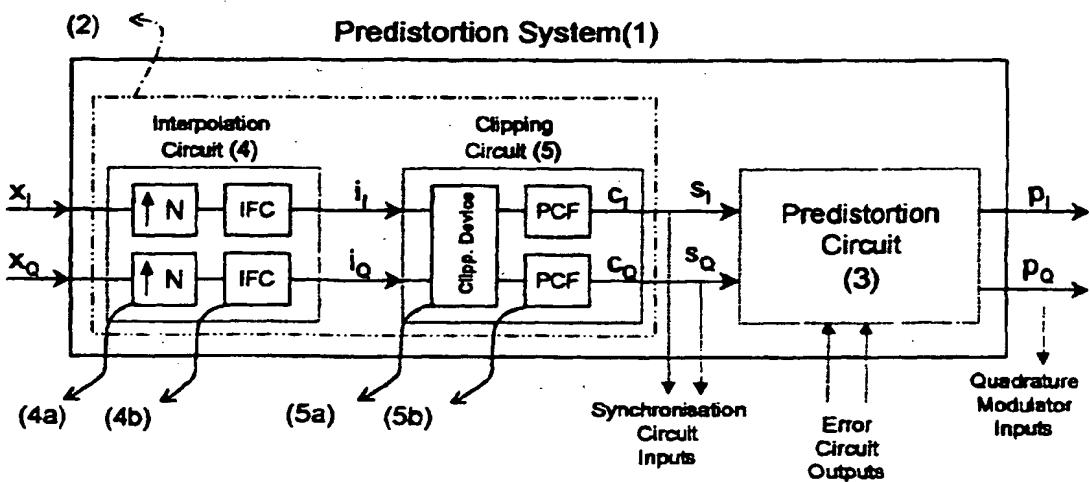


Fig. 2(a)

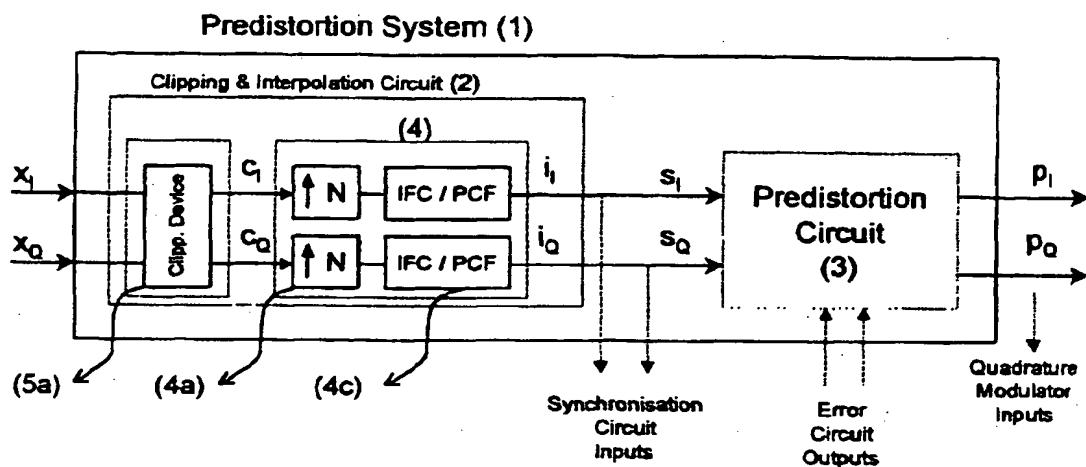


Fig. 2(b)

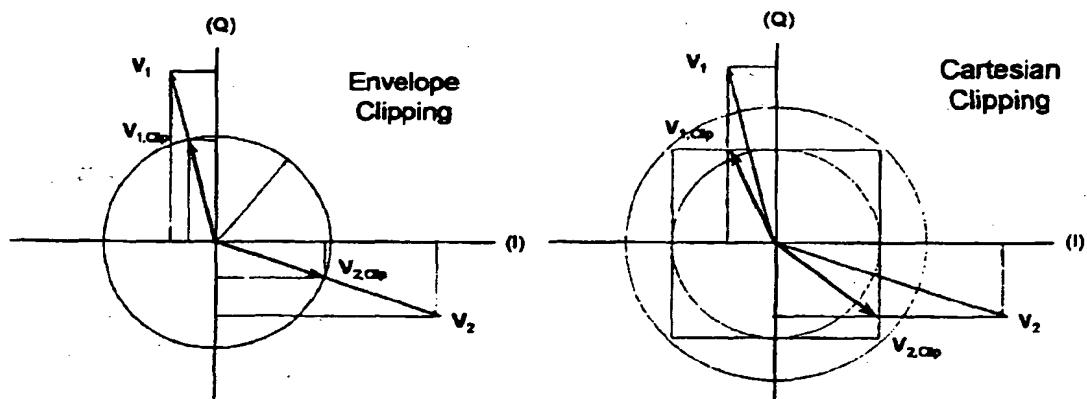


Fig. 3(a)

Fig. 3(b)

### Predistortion Circuit (3)

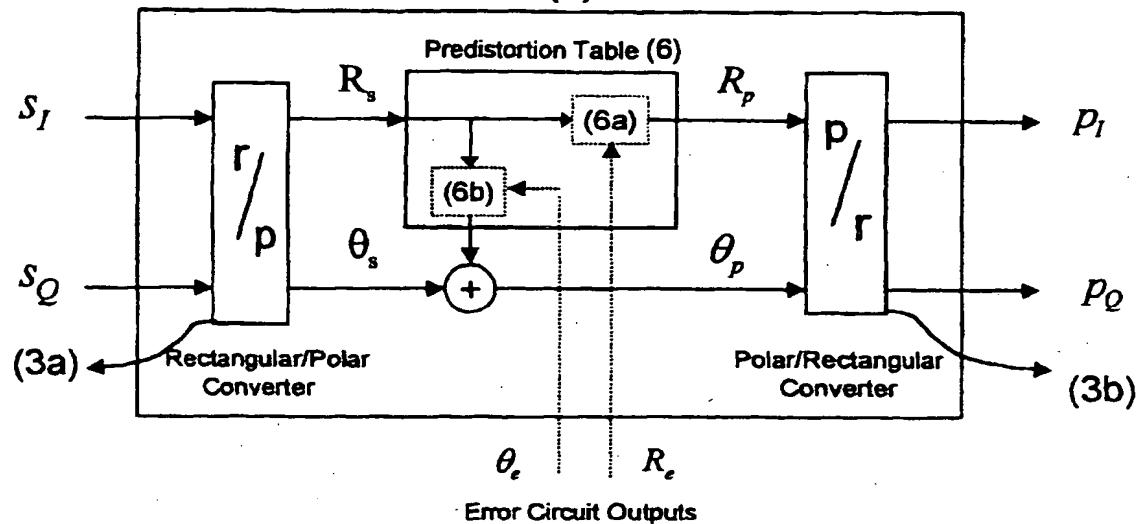


Fig. 4(a)

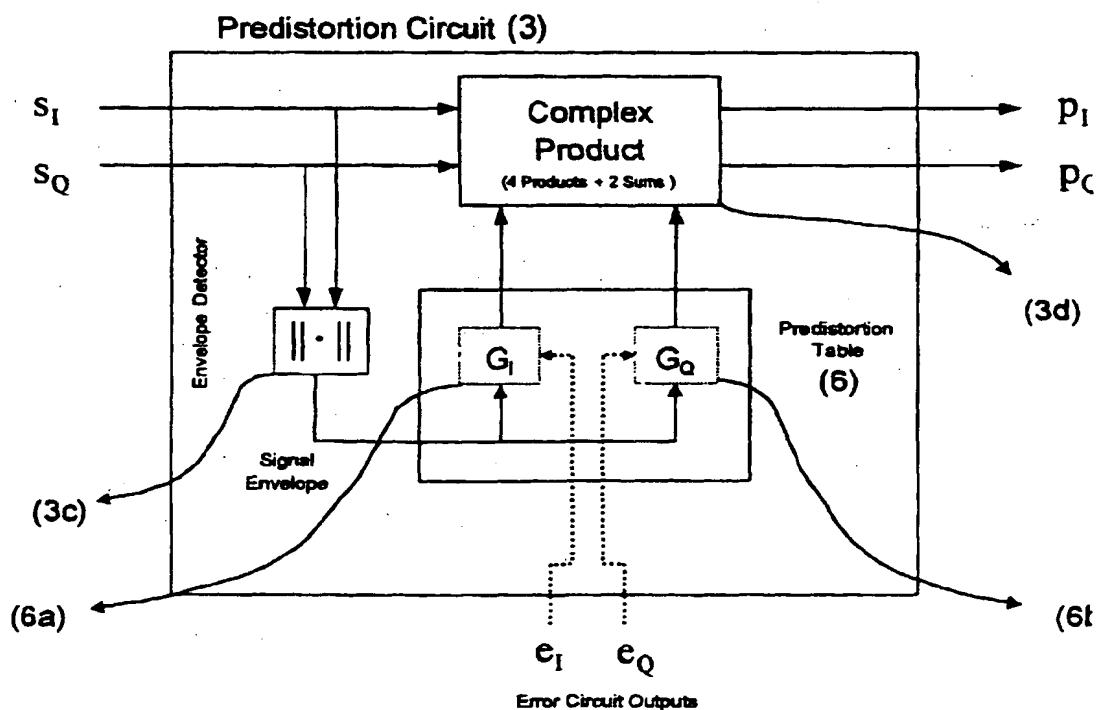
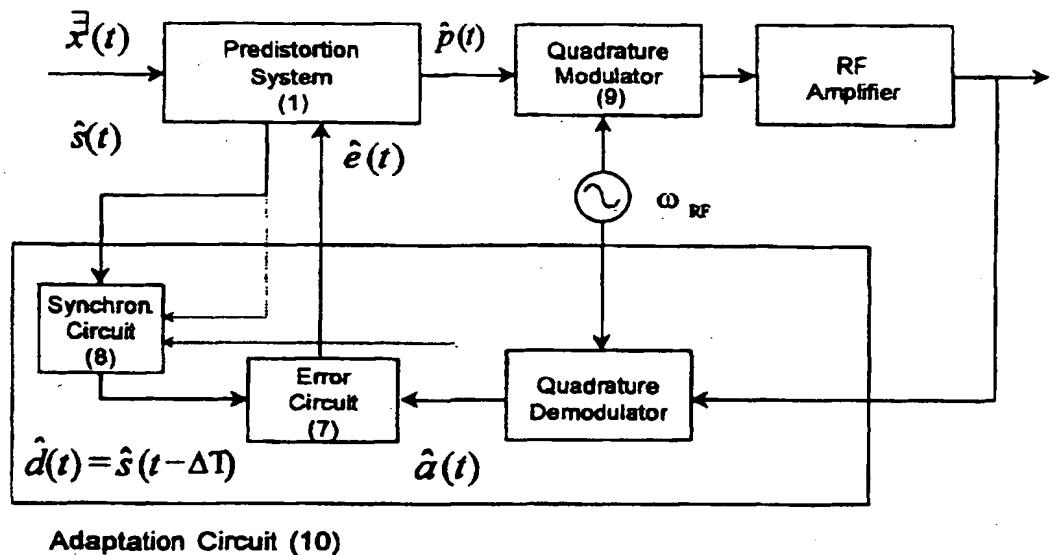
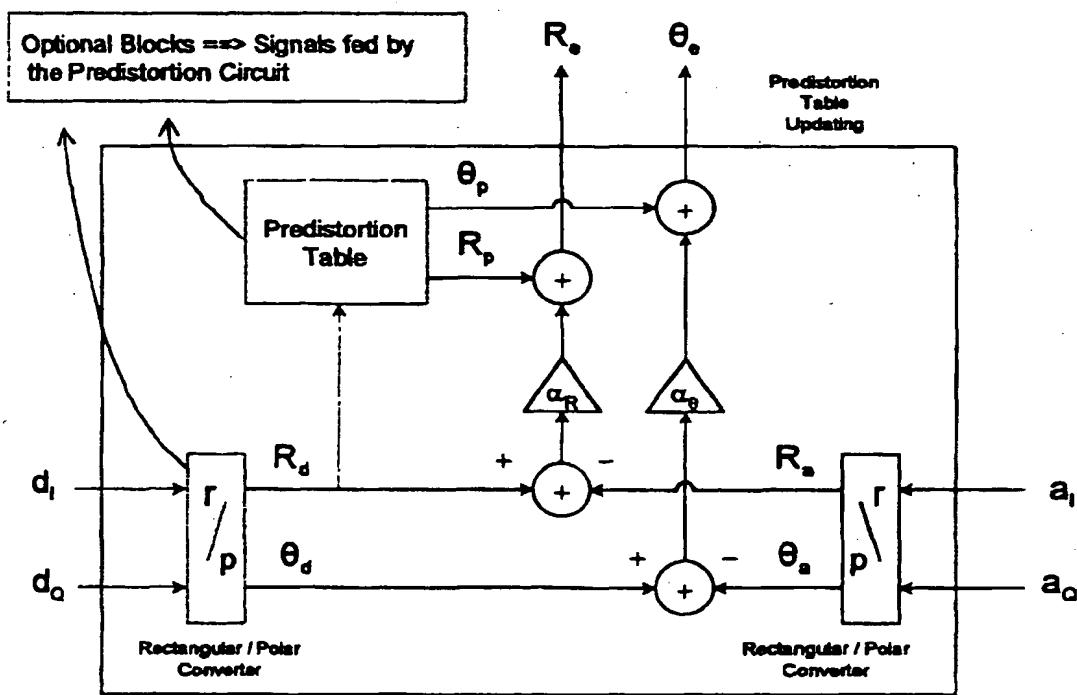


Fig. 4(b)



Adaptation Circuit (10)

Fig. 5



Error Circuit (7)

Fig. 6



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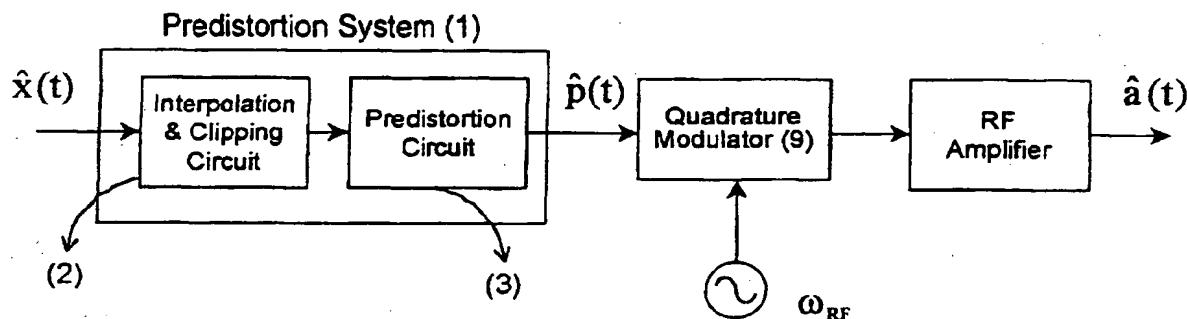


Fig. 1(a)



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## EUROPEAN SEARCH REPORT

Application Number

EP 00 83 0422

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A	* column 2, line 50 - line 65 * * column 5, line 4 - line 19; figure 2 *	5,13	
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The present search report has been drawn up for all claims			
Place of search	Date of completion of the search	Examiner	
MUNICH	8 July 2003	Marques, G	
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EP 00 83 0422

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